FORM PTO-1390 (Modified) (REV 11-98) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR
7616/16/1	09/647193

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/US99/06453	26 March 1999	27 March 1998

TITLE OF INVENTION
Method for Making Multilayer Thin-Film Electronics

APPLICANT(S) FOR DO/EO/US
Sigurd Wagner

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☐ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210).
8. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☐ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☒ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 20 below concern document(s) or information included:

13. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☐ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☒ Certificate of Mailing by Express Mail
20. ☒ Other items or information:

Verified Statement Claiming Small Entity Status

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/647193	PCT/US99/06453	7616/16/1

21. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☐	Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO and International Search Report not prepared by the EPO or JPO	**$970.00**
☐	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but Internation Search Report prepared by the EPO or JPO	**$840.00**
☐	International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO	**$690.00**
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) but all claims did not satisfy provisions of PCT Article 33(1)-(4)	**$670.00**
☒	International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(1)-(4)	**$96.00**

420 Rec'd PCT/PTO 27 SEP 2000

ENTER APPROPRIATE BASIC FEE AMOUNT =	**$96.00**	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☒ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	**$130.00**	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	22 - 20 =	2	x $18.00	**$36.00**	
Independent claims	4 - 3 =	1	x $78.00	**$78.00**	
Multiple Dependent Claims **(check if applicable)**.			☐	**$0.00**	
TOTAL OF ABOVE CALCULATIONS =				**$340.00**	
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) **(check if applicable).**			☒	**$170.00**	
SUBTOTAL =				**$170.00**	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)).			+	**$0.00**	
TOTAL NATIONAL FEE =				**$170.00**	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).**			☐	**$0.00**	
TOTAL FEES ENCLOSED =				**$170.00**	
				Amount to be: refunded	$
				charged	$

☐ A check in the amount of to cover the above fees is enclosed.

☒ Please charge my Deposit Account No. **06-2143** in the amount of $170.00 to cover the above fees.
A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **06-2143** A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Michael R. Friscia
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SIGNATURE

Michael R. Friscia
NAME

33,884
REGISTRATION NUMBER

9/27/00
DATE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Box: PCT
Assistant Commissioner for Patents
Washington, D.C. 20231

Re:	Our file:	7616/16/1	Examiner:
	Applicant:	Sigurd Wagner	Group Art Unit:
	Serial No.:	PCT/US99/06453	
	Filing Date:	26 March 1999	
	Title:	Method for Making Multilayer Thin-Film Electronics	

Sir:

Enclosed for filing in the United States Patent and Trademark Office is the following:

1. Transmittal Letter to the United States Designated/Elected Office (DO/EO/US) Concerning a Filing Under 35 U.S.C. 371
3. Copy of PCT International Application with Figures
4. Copy of International Search Report
5. Copy of International Preliminary Examination Report
5. Small Entity Statement
6. Transmittal Sheet
7. Postcard Receipt

CONDITIONAL PETITION

If any extension of time is required for the submission of the above-identified items, Applicant requests that this be considered a petition therefor. Please charge any additional charges or any other charges relating to this matter to deposit account of the writer, **Account No. 06-2143.** A duplicate copy of this letter is enclosed.

Respectfully submitted,

9/27/00
Date

Michael R. Friscia
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enc.

I hereby certify that this correspondence is being deposited with the United States Postal Service, postage prepaid, as "Express Mail Post Office to Addressee," Mailing Label No. EL548970705US to Box PCT, Assistant Commissioner for Patents, Washington, D.C. 20231 on 9/27/00.

By: _____
Michael R. Friscia

METHOD FOR MAKING MULTILAYER THIN-FILM ELECTRONICS

SPECIFICATION

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

This invention relates to large-area electronics and to methods for manufacturing thin film electronics continuously on separate carrier substrate foils, and then to combining these foils using anisotropic electrical conductors or light guides.

RELATED ART

In the field of thin film electronics where two or more layers of active circuits are employed, many technologies exist for connection of separate planes of passive circuits. One of these technologies is multilevel metallization on top of integrated silicon circuits, for which several levels of metal lines are built up by alternating between the fabrication of metal patterns, the deposition of insulators, the opening of vertical connections, followed by the fabrication of the next level of metal pattern, etc. Another of these technologies is multilevel printed wire boards (PWBs), for which passive metal connections are deposited on epoxy-based or ceramic boards that are fabricated with openings to make vertical connections. Individual boards are bonded to each other to form multilevel PWBs by bonding techniques that depend on the material of the board. These techniques are used industrially.

However, there are drawbacks associated with these existing techniques.

OBJECTS AND SUMMARY OF THE INVENTION

It is an object of this invention to provide a method of manufacturing macroelectronic circuits.

It is a further object of this invention to provide a method of manufacturing macroelectronic circuits which results in low cost and high yield.

It is yet another object of this invention to provide a method for manufacturing electronic circuits in a continuous process.

It is still a further object of the invention to provide a method of manufacturing electronic circuits where thin film electronics are manufactured continuously on separate carrier substrate foils.

It is another object of the invention to provide a method of combining the separately manufactured foils.

It is a still further object of the invention to combine separately manufactured foils using adhesives and anisotropic electrical conductors or light guides.

The present invention maintains high-speed manufacturing while the various component functions are manufactured separately under conditions tailored to optimize component performance and yield. The method involves the production of each function or group of functions on a separate flexible substrate, and bonding these flexible substrates to each other by using anisotropic electrically conducting or optical lightguide adhesives. The bonding is performed by laminating the flexible substrates to each other via the adhesive in a continuous process. Anisotropic conductors conduct in one direction (i.e. top to bottom) but do not conduct sideways.

BRIEF DESCRIPTION OF THE FIGURES

FIG. 1 is a schematic drawing of a pixel for a display of organic light emitting diodes driven by an active matrix of thin film transistors made on a steel back plane.

FIG. 2 is a diagram of a co-laminated thin film transistor using anisotropic electrically conducting adhesive.

DETAILED DESCRIPTION OF THE INVENTION

Many electronic products combine several electronic and/or optical functions. An active-matrix liquid-crystal display is an example of such a product. It consists of a light source, a plane of transistor electronics, a layer of liquid crystal sandwiched between transparent conductors and polarizers, and a plane of color filters. Typically, such products are made by separately manufacturing the individual components, such as the light source, the transistor back plane, and the color filter plane, followed by assembly and filling of the liquid crystal material. The separate manufacture allows the individual optimization of the performance of each component. Often, separate manufacture is necessary to obtain the desired functionality. For example, the transistor back plane of a liquid crystal display could not be manufactured after assembly, because assembly renders the required substrate surface inaccessible. However, it is well known that integration of several functions on one substrate leads to savings in cost, improvement of yield, and increased functionality.

The need for combining several electronic functions at low cost with high yield becomes paramount in the field of macroelectronics, also called large-area electronics or giant electronics. Macroelectronic products are expected to have very low cost per unit area, rather than per function as is the case for conventional microelectronics. This requirement is apparent for typical examples of future macroelectronic products, such as disposable, intelligent shipping/shopping labels, digital wallpaper, and dial-your-pattern dresses. These products may include transistor electronics, input/output devices such as antennae, optoelectronic functions including photodetectors and light-emitting diodes, and microelectromechanical devices.

To keep costs low and achieve high yield, the manufacture of macroelectronic products must combine high-speed production of these functions with their integration at high yield. High-speed production can be achieved by the printing of macroelectronics on flexible substrates. The substrate will spool off a roll, run through equipment that is configured like a multi-color printing press, and then will be coiled up or cut into product. The diversity of

macroelectronic component functions (transistors, LEDs, photodetectors, etc.) requires diverse materials and manufacturing processes. Superposing these materials and processes in a fully integrated sequence reduces yield because the temperature and chemicals required for producing a given function may damage a function that was introduced earlier in a lower layer of the multilayer structure.

The present invention maintains high-speed manufacturing while the various component functions are manufactured separately under conditions tailored to optimize component performance and yield. The basic concept is to produce each function or group of functions on a separate flexible substrate, and to bond these flexible substrates to each other by using anisotropic electrically conducting or optical lightguide adhesives. The bonding is performed by laminating the flexible substrates to each other via the adhesive in a continuous process.

FIG. 1 shows a pixel for a display of organic light emitting diodes driven by an active matrix of thin film transistors made on a steel back plane. In such devices, thin film transistors must make good electrical contact to the OLEDs to provide sufficient drive current. This is an active matrix emissive display which consists of a back plane of thin film transistors that drive organic light emitting diodes. Such a pixel is shown in the paper by Wu, et al. *Integration of Organic LEDs and Amorphous TFTs onto Unbreakable Metal Foil Substrates,* published in the Tech. Digest Internat. Electron Devices Meeting, San Francisco, CA, December 8011, 1996, IEEE, Piscataway, NJ 1996, Paper 308.1, pp. 957-959.

The display shown in FIG. 1 is manufactured in a sequence of steps that adds the TFT and OLED layers to one substrate. A substrate foil, for example, stainless steel, has patterned TFT circuits added first. The OLED circuits are then placed on the substrate. A transparent encapsulation layer (not shown) is then applied. The top contact to the OLED layer must be transparent to transmit the light, which is emitted from the organic semiconductor. In this structure this contact is made in one of the last processing steps. It was found experimentally

that this transparent contact to the OLED functions best when made first, i.e., when the OLED is made on top of it ("*Organic LEDs integrated with a-Si TFTs on lightweight metal substrates*", C.C. Wu, et al., Society for Information Display, Internat. Symp. Digest, Vol. XXVIII, SID, Santa Ana, CA 1997, pp. 67-70). However, making the OLEDs first on a transparent substrate, followed by making the TFTs on top of the OLEDs is not possible, because the typical TFT process temperature of 200° to 350° C will destroy the OLED, which must not be heated much above room temperature.

The present invention addresses this problem by making the TFT back plane and the OLEDs separately, and connecting them electrically with an anisotropic conductor, which conducts only in the direction perpendicular to the layers. This sequence of steps is illustrated in FIG. 2. More particularly, the OLED's 6 are formed on a transparent conductor 4 which is, in turn formed onto a transparent substrate/encapsulation 2. The back plane comprises thin film transistors (TFT's) formed onto structural substrate 10. When the substrate 10 is conducted as is the case for metal foils, an insulated barrier layer 12 must be deposited between the TFT layer and the substrate. The front plane OLED's and the back plane TFT's are connected together with an anistropic conductive adhesive 8. The resultant structure is the finished thin film display.

Nothing is changed in TFT manufacture as compared to the sequence described above. However, the OLEDs are made on a transparent conductor, which in turn is deposited on a transparent substrate. In this way, the best possible electrical contact to the OLEDs is made, and the transparent substrate ultimately serves as the transparent encapsulant. The other electrical contact to the OLEDs may be opaque and is made of a suitable metal. The two planes, TFT and OLED, are then laminated to each other, using an adhesive foil of anisotropic conductor (for example, ARclad® 8257 from Adhesives Research, Inc., a 1-mil thick acrylic product). The final assembly step therefore is the co-lamination of TFT foil, anisotropic conductor foil, and OLED foil.

It is important to note that the proper TFT-OLED connections are made automatically by this procedure, as long as the TFT and OLED planes are

aligned with each other.

The same principle can be used to co-laminate component planes with anisotropic light guides, if optical interconnects are desired. The lamination step may be repeated to combine more than two active planes in one product.

Having a body of easily deformable adhesive also provides another advantage in production yield and product lift. The anisotropic conductor will accommodate mechanical strain between the circuit planes that it connects. If a rigid connection were used, any strain developing during fabrication or in produce use will be accommodated by the layer with the lowest elastic modulus. This may be an active layer, for example, the organic light-emitter. Straining this layer may destroy the OLED. Straining the adhesive layer will only lead to local shifts in the contact alignment, which will be self-correcting due to the anisotropic conduction or light guiding.

Anisotropic conductors are used today to make connections between groups of passive conductors on to different planes. One well-known application is the surface-mount of integrated driver circuits to the row and column conductors of liquid crystal displays. The use of a sheet of an anisotropically conducting adhesive for the direct connection of two active circuit planes is new. The problem solved here is coming into being only now, as macroelectronic integrated circuits are developed.

While several advantageous embodiments have been chosen to illustrate the invention, it will be understood by those skilled in the art that various changes and modifications can be made therein without departing from the scope of the invention as defined in the appended claims.

Having thus described the invention in detail, it is to be understood that the foregoing description is not intended to limit the spirit and scope thereof. What is desired to be protected by Letters Patent is set forth in the appended claims.

CLAIMS

What is claimed is:

1. A process for manufacturing macroelectronics comprising the steps of: producing thin film active electronics on separate carrier substrates; and combining said substrates using anisotropic electrical conductors or light guides.

2. The process of claim 1 wherein one of said substrates is a flexible foil.

3. The process of claim 1 wherein one of said substrates is a rigid plate.

4. The process of claim 2 wherein the material for one of said substrates is plastic.

5. The process of claim 3 wherein the material for one of said substrates is plastic.

6. The process of claim 2 wherein the material for one of said substrates is glass.

7. The process of claim 3 wherein the material for one of said substrates is glass.

8. The process of claim 2 wherein the material for one of said substrates is metal.

9. The process of claim 3 wherein the material for one of said substrates is metal.

10. The process of claim 1 wherein the thin film active electronics are producted continuously on seperate carrier substrates.

11. The process of claim 4 wherein organic light emitting diodes are formed on the plastic substrate.

12. The process of claim 5 wherein organic light emitting diodes are formed on the plastic substrate.

13. The process of claim 6 wherein organic light emitting diodes are formed on the glass substrate.

14. The process of claim 7 wherein organic light emitting diodes are formed on the glass substrate.

15. The process of claim 6 wherein thin film transistors are formed on the glass substrate.

16. The process of claim 7 wherein thin film transitors are formed on the glass substrate.

17. A process of making electronic circuits comprising the steps of:

forming at least two active circuits on separate carrier substrates; and

combining said active circuits by connecting them with a material which conducts in only a single direction.

18. A method of manufacturing an electronic display comprising the steps of:

depositing a transparent conductor on a transparent substrate;

forming a thin film organic light emitting diode circuit on said transparent conductor;

forming a thin film transistor circuit; and

laminating said circuits to each other.

19. The method of claim 18 wherein said laminating step uses an adhesive anisotropic conductor.

20. The method of claim 19 wherein the conductor is an electrical or optical conductor.

21. The method of claim 19 wherein the bonding layer is the conductor.

22. A method of manufacturing an electronic circuit comprising the steps of:

forming a first active circuit on a first plane;

forming a second active circuit on a second plane; and

co-laminating said first and second planes with an anisotropic conductor in between.

FIG. 1

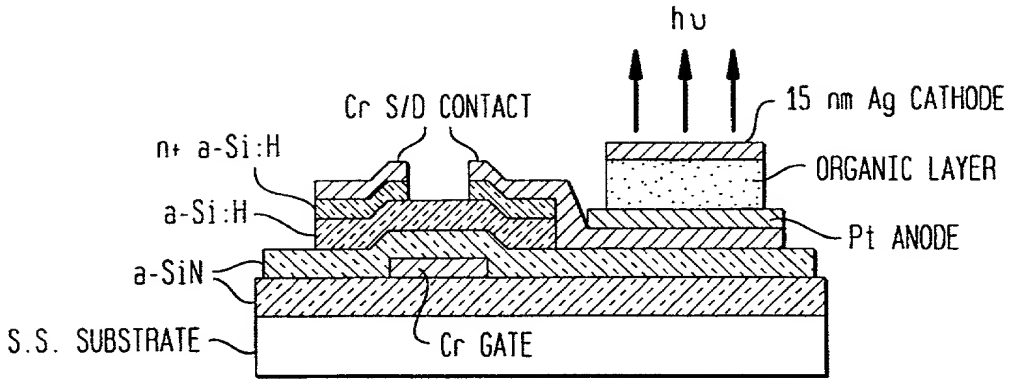
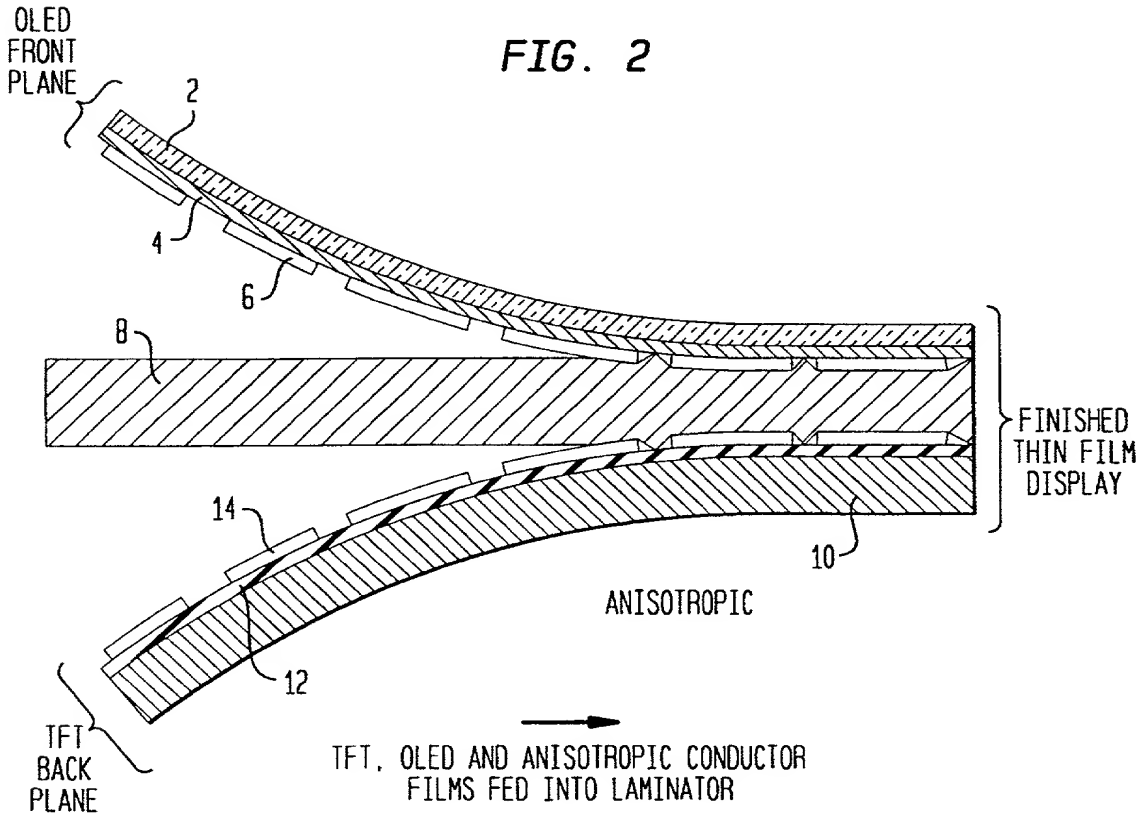

hυ
Cr S/D CONTACT
15 nm Ag CATHODE
n+ a-Si:H
ORGANIC LAYER
a-Si:H
Pt ANODE
a-SiN
S.S. SUBSTRATE
Cr GATE

FIG. 2


OLED FRONT PLANE
2
4
6
8
FINISHED THIN FILM DISPLAY
14
10
ANISOTROPIC
12
TFT BACK PLANE
TFT, OLED AND ANISOTROPIC CONDUCTOR FILMS FED INTO LAMINATOR

Docket No.
7616/16/1

Declaration and Power of Attorney For Patent Application

English Language Declaration

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
Method for Making Multilayer Thin-Film Electronics

the specification of which

(check one)

☐ is attached hereto.

☒ was filed on **March 26, 1999** as United States Application No. or PCT International Application Number **PCT/US99/06453**

and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d) or Section 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Not Claimed
(Number)	(Country)	(Day/Month/Year Filed)	☐
(Number)	(Country)	(Day/Month/Year Filed)	☐
(Number)	(Country)	(Day/Month/Year Filed)	☐

I hereby claim the benefit under 35 U.S.C. Section 119(e) of any United States provisional application(s) listed below:

60/079,746	03/27/98
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)
(Application Serial No.)	(Filing Date)

I hereby claim the benefit under 35 U. S. C. Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. Section 112, I acknowledge the duty to disclose to the United States Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, C. F. R., Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)
(Application Serial No.)	(Filing Date)	(Status) (patented, pending, abandoned)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

Michael R. Friscia
Registration No. 33,884 (1)

Send Correspondence to: **Michael R. Friscia**
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Direct Telephone Calls to: *(name and telephone number)*
Michael R. Friscia (973) 533-6599

(1 of 2)

Full name of sole or first inventor **Sigurd Wagner**
Sole or first inventor's signature: Sigurd Wagner Date: 9/27/2000
Residence **16 Malcom Circle, Princeton, NJ 08540** NJ
Citizenship **USA**
Post Office Address **16 Malcom Circle, Princeton, NJ 08540**

Full name of second inventor, if any
Second inventor's signature Date
Residence
Citizenship
Post Office Address

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9(f) AND 1.27 (d)) - NONPROFIT ORGANIZATION	Docket No. 7616/16/1

Serial No.	Filing Date	Patent No.	Issue Date

Applicant/ Patentee: **Sigurd Wagner**

Invention: **Method for Making Multilayer Thin-Film Electronics**

I hereby declare that I am an official empowered to act on behalf of the nonprofit organization identified below:

NAME OF ORGANIZATION: **The Trustees of Princeton University**

ADDRESS OF ORGANIZATION: **Princeton University**
P.O. Box 36
Princeton, NJ 08544-0036

TYPE OF NONPROFIT ORGANIZATION:

- ☒ University or other Institute of Higher Education
- ☐ Tax Exempt under Internal Revenue Service Code (26 U.S.C. 501(a) and 501(c)(3))
- ☐ Nonprofit Scientific or Educational under Statute of State of The United States of America
  Name of State: Citation of Statute:
- ☐ Would Qualify as Tax Exempt under Internal Revenue Service Code (26 U.S.C. 501(a) and 501(c)(3)) if Located in The United States of America
- ☐ Would Qualify as Nonprofit Scientific or Educational under Statute of State of The United States of America if Located in The United States of America
  Name of State: Citation of Statute:

I hereby declare that the above-identified nonprofit organization qualifies as a nonprofit organization as defined in 37 C.F.R. 1.9(e) for purposes of paying reduced fees to the United States Patent and Trademark Office regarding the invention described in:

- ☒ the specification to be filed herewith.
- ☐ the application identified above.
- ☐ the patent identified above.

I hereby declare that rights under contract or law have been conveyed to and remain with the nonprofit organization with regard to the above identified invention.

If the rights held by the above-identified nonprofit organization are not exclusive, each individual, concern or organization having rights to the invention is listed on the next page and no rights to the invention are held by any person, other than the inventor, who could not qualify as an independent inventor under 37 CFR 1.9(c) or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey, or license any rights in the invention is listed below:

☒ no such person, concern or organization exists.
☐ each such person, concern or organization is listed below.

FULL NAME _____
ADDRESS _____
☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

FULL NAME _____
ADDRESS _____
☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

FULL NAME _____
ADDRESS _____
☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

FULL NAME _____
ADDRESS _____
☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING: **Allen J. Sinisgalli**

TITLE IN ORGANIZATION: **Associate Provost**

ADDRESS OF PERSON SIGNING: **Princeton University**
P.O. Box 36
Princeton, NJ 08544-0036

SIGNATURE: Allen J. Sinisgalli DATE: 9/21/00